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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,676	LIN ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-26 and 29-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 19-26 and 29-38 are pending and have been examined.

2. Claims 19-26 and 29-38 are rejected.

Response to Arguments

3. Applicant's arguments, see page 7 of the amendment filed August 29, 2006, with respect to the rejection(s) of claim(s) 19 and 29 under 35 U.S.C. § 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wilkie (U.S. 5,083,261). Applicant's allege, "Hewitt does not disclose or suggest...dynamically adjusting the first and second priority access values in response to a user request" in response to the Office Action's pointing to column 2, lines 38-40 of Hewitt that discloses "a set of programmable registers...provided to allow software programming of the initial count value." While Hewitt discloses the priority access values are dynamically adjustable through software programming, they do not explicitly disclose the software programming of priority access values is in response to a user request. The Examiner believes the software programming itself represents a user request to dynamically adjust the priority access values, however in an effort to advance prosecution the Wilkie reference will be used to show that a user request to dynamically alter the priority access value is well known in the art.

Claims 20-26 depend from claim 19 and will be rejected over Hewitt in view of Wilkie for the reasons listed above and further discussed below.

Claims 30-38 depend from claim 29 and will be rejected over Hewitt in view of Wilkie for the reasons listed above and further discussed below.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 19-20 and 22-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hewitt et al. (US005956493A) in view of Wilkie (US 5,083,261).

Hewitt discloses a method of managing a memory bus, the method comprising: receiving a first memory access request from a first request agent that represents a first functional device and a second memory access request from a second request agent that represents a second functional device (col. 3, line 61 – col. 4, line 10; Each requesting device has a unique REQ# signal); loading a first access priority value into a first counter timer, wherein the first access priority value corresponds to a processing function (As previously stated by the Examiner in the Office Action dated March 6, 2006, "In any priority based arbitration system the assignment of priorities to devices of a computer system is performed with regards to the severity of the function performed by a device (page 2)." "In other words a device that is given priority because it requires a larger bandwidth is given priority because the *processing function* of a particular device requires the larger bandwidth." The Hewitt supports this assertion by the Examiner when stating, "...real time bus masters which require quick access to the bus may be programmed with an initial count value (priority value) which is relatively low (indicating a higher priority)..." in

addition "...bus masters which can withstand longer latencies in obtaining the bus may be programmed with initial count values which are higher (indicating a lower priority) (col. 5, ll. 50-62)." Furthermore priorities may be assigned to bus masters, which each have their own processing function, "...based on various parameters..." including "bandwidth requirements... and to specify whether a particular master (i.e. processing function) is a real time or non-real time resource (col. 5, line 63 – col. 6, line 3).") that is provided by the first functional device (col. 4, ll. 30-53); loading a second access priority value into a second counter timer, wherein the second access priority value corresponds to a different processing function that is provided by the second functional device (col. 4, ll. 30-53); where the first functional device accesses a memory bus before the second functional device when the first access priority value represents a higher priority than the second access priority value (col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource.); and wherein the second functional device accesses the memory bus before the first functional device when the second access priority value represents a higher priority than the first access priority value (col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource.). While Hewitt discloses the priority access values are dynamically adjustable through software programming, they do not explicitly disclose the software programming of priority access values is in response to a user request.

Wilkie teaches a system and method for dynamically altering priority of interrupts/requests. "In more recent data processing systems, the flexibility of the interrupt mechanism has been enhanced by allowing the user to dynamically alter the relative priorities of the several interrupt

levels (col. 1, ll. 38-41)." As an improvement to the prior art systems Wilkie teaches providing "an interrupt priority circuit which enables the user to select the interrupt signal from a particular one of a plurality of resources which is to have the highest priority (col. 2, ll. 21-26)." In addition, Wilkie teaches "an interrupt priority circuit which allows the user to dynamically change the interrupt signal from a particular one of a plurality of resources so as to have the highest priority (col. 2, ll. 26-31)."

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the teachings of Wilkie into the bus arbitration system of Hewitt such that the user of the Hewitt system "may dynamically alter the relative priorities of several resources (Wilkie; col. 4, ll. 44-46)." The ability to dynamically alter access priorities allows the user of a computer system to influence resource assignment thus providing the ability to customize system performance to meet specific tasks or requirements.

For claim 19 Hewitt in view of Wilkie teach:

A method of managing a memory bus, the method comprising:

- Receiving a first memory access request from a first request agent that represents a first functional device and a second memory access request from a second request agent that represents a second functional device (Hewitt; col. 3, line 61 – col. 4, line 10; Each requesting device has a unique REQ# signal);
- Loading a first access priority value into a first counter timer, wherein the first access priority value corresponds to a processing function (Hewitt; As previously stated by the

Examiner in the Office Action dated March 6, 2006, "In any priority based arbitration system the assignment of priorities to devices of a computer system is performed with regards to the severity of the function performed by a device (page 2)." "In other words a device that is given priority because it requires a larger bandwidth is given priority because the *processing function* of a particular device requires the larger bandwidth." The Hewitt supports this assertion by the Examiner when stating, "...real time bus masters which require quick access to the bus may be programmed with an initial count value (priority value) which is relatively low (indicating a higher priority)..." in addition "...bus masters which can withstand longer latencies in obtaining the bus may be programmed with initial count values which are higher (indicating a lower priority) (col. 5, ll. 50-62)." Furthermore priorities may be assigned to bus masters, which each have their own processing function, "...based on various parameters..." including "bandwidth requirements... and to specify whether a particular master (i.e. processing function) is a real time or non-real time resource (Hewitt; col. 5, line 63 – col. 6, line 3).") that is provided by the first functional device (Hewitt; col. 4, ll. 30-53);

- Loading a second access priority value into a second counter timer, wherein the second access priority value corresponds to a different processing function that is provided by the second functional device (Hewitt; col. 4, ll. 30-53);
- Dynamically adjusting the first priority access value and the second priority access value in response to a user request (Wilkie; col. 1, ll. 38-41;col. 2, ll. 21-31), wherein the first priority access value and the second priority access value are stored in a control register (Hewitt; Fig. 2, 212; col. 4, ll. 45-53);

- Where the first functional device accesses a memory bus before the second functional device when the first access priority value represents a higher priority than the second access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource.); and
- Wherein the second functional device accesses the memory bus before the first functional device when the second access priority value represents a higher priority than the first access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource.).

For claim 20 Hewitt in view of Wilkie teach:

The method of claim 19, wherein a bus elector compares the first access priority value to the second access priority value (Hewitt; Fig. 2, 202; col. 4, line 54 – col. 5, line 13).

For claim 22 Hewitt in view of Wilkie teach:

The method of claim 19, wherein the first access priority value represents the higher priority when the first access priority value is lower than the second access priority value (Hewitt; col. 4, line 11 – col. 5, line 20).

For claim 23 Hewitt in view of Wilkie teach:

The method of claim 22, further comprising:

- Starting a first clock cycle when the first functional device accesses the memory bus; and decrementing the second access priority value after the first clock cycle has expired

(Hewitt; As previously stated in the Office Action dated October 28, 2005 the counters of Hewitt are updated on a clock cycle basis such that the level of arbitration priority is increased as a function of time. Therefore the priority values of devices not granted access to the system resource are decremented (increased in priority). Col. 4, ll. 1ine – col. 5, line 20).

For claim 24 Hewitt in view of Wilkie teach:

The method of Claim 23, further comprising:

- Receiving a third memory access request from a third request agent that represents a third functional device (Hewitt; col. 3, line 61 – col. 4, line 10; Each requesting device has a unique REQ# signal);
- Loading a third access priority value into a third counter timer, wherein the third access priority value corresponds to another processing function that is provided by the third functional device (Hewitt; col. 4, ll. 30-53);
- Wherein the second functional device has priority access to the memory bus when the decremented second access priority value represents a higher priority than the third access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource. Furthermore counters are decremented to insure fairness [col. 5, ll. 14-20].); and
- Wherein the third functional device has priority access to the memory bus when the third access priority value represents a higher priority than the decremented second access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority

is granted access to the resource. Furthermore counters are decremented to insure fairness [col. 5, ll. 14-20].).

For claim 25 Hewitt in view of Wilkie teach:

The method of claim 24, further comprising:

- Decrementing the third access priority value, when the second functional device accesses the memory bus and a second clock cycle ends (Hewitt; col. 5, ll. 14-20);
- Receiving a next memory request from the second request again (Hewitt; col. 5, ll. 19-20, "if the master reasserts its bus request signal");
- Resetting the decremented second has priority access to priority value to the second access priority value (Hewitt; col. 5, ll. 16-19); and
- Wherein the second functional device has priority access to the memory bus when the second access priority value represents a higher priority than the decremented third access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource. Furthermore counters are decremented to insure fairness [col. 5, ll. 14-20].); and
- Where the third functional device accesses the memory bus when the decremented third access priority value represents a higher priority than the second access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource. Furthermore counters are decremented to insure fairness [col. 5, ll. 14-20].).

For claim 26 Hewitt in view of Wilkie teach:

The method of claim 19, further comprising:

- Determining whether the memory bus is locked; and preventing the first functional device and the second functional device from accessing the memory bus when the memory bus is locked (Hewitt; col. 6, ll. 15-22).

For claim 29 Hewitt in view of Wilkie teach:

A system to manage a memory bus, the system comprising:

- A memory bus (Hewitt; Fig. 1, 120) configured to communication with a first functional device (Hewitt; Fig. 1, devices 122, 140, 170, 172, 174 and 176; col. 3, ll. 39-51) that provides a first processing function and with a second functional device that provides a second processing function (Hewitt; Fig. 1, devices 122, 140, 170, 172, 174 and 176; col. 3, ll. 39-51);
- Wherein the first functional device is represented by a first request agent and the second functional device is represented by a second request agent (Hewitt; col. 3, line 61 – col. 4, line 10; Each requesting device has a unique REQ# signal);
- A control register configured to store a first access priority value associated with the first request agent and a second access priority value associated with the second request agent (Hewitt; Fig. 2, 212; col. 4, ll. 45-53);
- Wherein the first access priority value corresponds to the first processing function and the second access priority value corresponds to the second processing function (Hewitt; As

previously stated by the Examiner in the Office Action dated March 6, 2006, "In any priority based arbitration system the assignment of priorities to devices of a computer system is performed with regards to the severity of the function performed by a device (page 2)." "In other words a device that is given priority because it requires a larger bandwidth is given priority because the *processing function* of a particular device requires the larger bandwidth." The Hewitt supports this assertion by the Examiner when stating, "...real time bus masters which require quick access to the bus may be programmed with an initial count value (priority value) which is relatively low (indicating a higher priority)..." in addition "...bus masters which can withstand longer latencies in obtaining the bus may be programmed with initial count values which are higher (indicating a lower priority) (Hewitt; col. 5, ll. 50-62)." Furthermore priorities may be assigned to bus masters, which each have their own processing function, "...based on various parameters.:." including "bandwidth requirements... and to specify whether a particular master (i.e. processing function) is a real time or non-real time resource (Hewitt; col. 5, line 63 – col. 6, line 3)."; *also see col. 6, ll. 23-30*);

- Wherein the control register is configured to dynamically adjust the first priority access value and the second priority access value in response to a user request (Wilkie; col. 1, ll. 38-41; col. 2, ll. 21-31)
- A control unit (Hewitt; Fig. 1 &2, 180) configured to load the first access priority value into a first counter timer when the first request agent issues a first memory access request, and to load the second access priority value into a second counter timer when the second

request agent issues a second memory access request (Hewitt; col. 4, line 23 – col. 6, line 22);

- Wherein the first functional device accesses the memory bus before the second functional device when the first access priority value represents a higher priority than the second access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource.); and
- Wherein the second functional device accesses the memory bus before the first functional device when the second access priority value represents a higher priority than the first access priority value (Hewitt; col. 4, line 54, col. 5, line 13; The device with the highest priority is granted access to the resource.).

For claim 30 Hewitt in view of Wilkie teach:

The system of claim 29, wherein the first memory access request and the second memory access request are received by a bus arbiter (Hewitt; col. 3, line 61 – col. 4, line 10).

For claim 31 Hewitt in view of Wilkie teach:

The system of claim 29, further comprising a bus elector coupled to the first counter timer and the second counter timer, wherein the bus elector is configured to compare the first access priority value to the second access priority value (Hewitt; Fig. 2, 202; col. 4, line 54 – col. 5, line 13).

For claim 32 Hewitt in view of Wilkie teach:

The system of claim 29, wherein the first functional device and the second functional device are included within a moving picture experts group (MPEG) video codec processor (Hewitt; col. 6, ll. 23-30).

For claim 33 Hewitt in view of Wilkie teach:

The system of claim 29, further comprising a control unit coupled to the request agents for respectively receiving corresponding request for access to the memory bus (Hewitt; Fig. 1 & 2, 180; col. 4, line 23 – col. 6, line 22).

For claim 34 Hewitt in view of Wilkie teach:

The system of claim 29, wherein the first functional device and the second functional device are selected from a group consisting of memory controller, image processors, motion estimation processors, and host/peripheral interfaces (Hewitt; col. 6, ll. 23-30; col. 3, line 39 – col. 4, line 10).

For claim 35 Hewitt in view of Wilkie teach:

The system of claim 29, wherein the first access priority value represents a first maximum latency count and the second access priority value represent a second maximum latency count (Hewitt; col. 4, line 11 – col. 5, line 20).

For claim 36 Hewitt in view of Wilkie teach:

The system of claim 29, further comprising a plurality of clocks that time a clock cycle when the memory bus is accessed (Hewitt; Col. 4, ll. 1ine – col. 5, line 20; col. 6, ll. 15-22).

For claim 37 Hewitt in view of Wilkie teach:

The system of claim 36, further comprising a bus release mechanism, wherein the plurality of clocks begin the clock cycle when the bus release mechanism releases the first functional device or the second functional device to access the memory bus (Hewitt; Col. 4, ll. 1ine – col. 5, line 20; col. 6, ll. 15-22).

For claim 38 Hewitt in view of Wilkie teach:

The system of claim 36, further comprising a bus release mechanism, wherein the bus release mechanism releases the first functional device or the second functional device to access the memory bus after at least one of the plurality of clocks begin to time the clock cycle (Hewitt; Col. 4, ll. 1ine – col. 5, line 20; col. 6, ll. 15-22).

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hewitt in view of Wilkie and further in view of what was well known in the art at the time of applicant's invention.

The Examiner has previously shown that the invention of Hewitt selects competing requests on the basis of the smallest counter value representing a highest priority. Subtracting one from the current priority grade value of all denied sources dynamically alters the priority grade. OFFICIAL NOTICE is taken that it would have been obvious to one of ordinary skill in the pertinent art to add one to the initial priority grade values instead of subtracting one. The addition of one to all denied sources and the selection of the largest priority grade is functionally equivalent to subtracting one from all denied sources and selecting the competing source with the smallest priority grade. The Examiner respectfully submits that there is no significant novelty in implementing an addition/selecting largest priority value scheme over a subtraction/selecting smallest priority value scheme since the two schemes are functionally equivalent.

It is noted that the common knowledge or well-known in the art statement (subtraction/selecting smallest priority value scheme) is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate. In this instance applicant merely alleges claim 21 is allowable because it depends from claim 19 to which applicant argues is allowable and has not challenged the Examiner's use of Official Notice. *Please see MPEP §2144.03.*

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yishay also teaches a user request to adjust priority is well known in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RMS

PAUL R. MYERS
PRIMARY EXAMINER